Modern Power Semiconductor Devices (A Review)

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Abstract: This paper discusses the different types of power semiconductor devices. It also describes the operation, characteristics and applications of different devices. The principle of operation and the key features of different devices is discussed. The other thyristor group devices, such as Triac having capability to conduct in both positive and negative half of ac supply and GTO with facility to turn-on and turn-off from the gate were made commercially available in 1960s.

The power Static Induction Transistor (SIT) in modern form was commercially introduced by Tokin Corporation of Japan in 1987. Its conduction drop is very large but switching frequency is very high. A Static Induction Thyristor (SITH) is a self controlled GTO.General Electric announced a MOS-Controlled Thyristor (MCT)which is a high power, high frequency GTO like device with MOS-gated turn-on and turn-off characteristics.

Index terms: BJT – Bipolar Junction Transistor,GTO - Gate Turn Off Thyristor, SCR - Silicon controlled Thyristor, SIT – Static Induction Transistor, MCT – Mos Controlled Thyristor

1. INTRODUCTION:

Power semiconductor device is the heart of modern power electronics. It operates as a switch When the device conducts, it behaves as an ordinary closed switch. Therefore, ideally no voltage drop occurs across the device and the supply voltage applies to the load. Similarly, when the device does not conduct, it behaves as opened switch and offers ideally an infinite impedance. The load circuit gets disconnected and no load current flows from the source to the load.

The silicon material is widely used for the fabrication of power semiconductors. It will take long way to replace silicon when the technology of these materials advances

2. CLASSIFICATION OF SEMICONDUCTOR DEVICES:

The power semiconductor devices can be classified on the basis of:

1. Uncontrolled turn-on and turn-off (Diode)
2. Controlled turn-on and uncontrolled turn-off (SCR, TRIAC)
3. Controlled turn-on and controlled turn-off (BJT, MOSFET, COOLMOS, IGBT, SIT, GTO, IGCT, MCT, SITH)
4. Continuous gate signal requirement (BJT, MOSFET, COOLMOS, IGBT, SIT)

3. DESIRABLE CHARACTERISTICS OF SEMICONDUCTOR DEVICES:

1. **On-state characteristics**
   - (i) High current rating
   - (ii) Low forward voltage drop
2. **Off-state characteristics**
   - (i) High forward and reverse voltage blocking capability
   - (ii) Low leakage current
3. **Switching characteristics**
   - (i) Low and controllable turn-on and turn-off time
   - (ii) High dv/dt and di/dt rating
   - (iii) Low switching power losses

4. **Gate characteristics**
   - (i) Low gate-drive voltage and low gate-drive current
   - (ii) Low gate drive power

5 Fault withstanding capability
- (i) High value of i^2t to withstand fault current for a long time.

6. Thermal stability.
- (i) Low thermal impedance from the internal junction to the ambient coefficient

4. BASIC DESCRIPTION OF MODERN POWER DEVICES:

The power semiconductor devices have been grouped into following two categories:

- (i) The old or conventional devices i.e. power diode, thyristor, TRIAC, GTO, BJT and power MOSFET.
- (ii) Modern power devices i.e. IGBT, SIT, SITH, MCT, IGCT and COOLMOS etc.

4.1 Power MOSFET

The Power MOSFET (Metal Oxide Semiconductor Field Effect Transistor was evolved from integrated circuit technology in response to the need to develop power transistors that can be controlled using much lower gate drive power levels as compared to the existing power transistors. A power MOSFET is a unipolar voltage controlled device and requires very small gate current for its turn on.

Basic Structure of n-channel MOSFET

A power MOSFET, like a power transistor, is a three terminal device having source, gate and drain terminals. The n^+ p n^{-1} n^+ is termed an enhancement mode n-channel MOSFET because it does not have depletion mode The enhancement type MOSFET remains off at zero gate voltage, hence generally used as a switching device in power electronics. Figure 1(a) shows device symbol for n-channel power MOSFET.

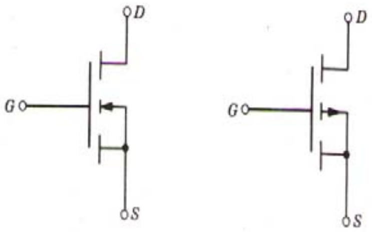


Fig 1(a) Device symbol

Operation and Static Characteristics:

When no gate source voltage (V_{GS}) is applied, the device remains in off position (cut-off) because of no conduction channel is available even if positive drain source voltage (V_{DS}) is applied below the breakdown voltage. If a small positive V_{GS} is applied to the device shown in figure 2(a), the positive charge is induced on the upper metallization. This electric field from the positive charge repels the majority carrier holes from the interface region in p-base, thereby, a depletion region is created. The negatively charged acceptors balance the induced positive charge. Further increases in V_{GS} cause the depletion layer to grow in thickness as shown in Figure 2(b As the voltage V_{GS} is increased, the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as well as repelling free holes. The free holes being pushed into the p-base ahead of depletion region.As the voltage V_{GS} is further increased, the density of free holes at the interface region becomes even greater than the free hold density in the p-base region away from the depletion region and the layer of free electrons at the interface will be highly conducting as n-type semiconductor. The resulting surface electron layer provides a path between the N^+ source region and the N^- drift region. This layer of free electrons is termed as the inversion layer. The field effect enhances the conductivity of the interface and hence, the name enhancement mode field effect transistor. The value of V_{GS} at which the inversion layer is formed is termed as the threshold voltage V_{GS}(th). As the V_{GS} is increased beyond V_{GS}(th), the inversion layer gets thicker and more conductive as the density of free electrons increases. The depletion layer thickness adjacent to the inversion layer now remains constant even V_{GS} further increases shown in figure 2(c).

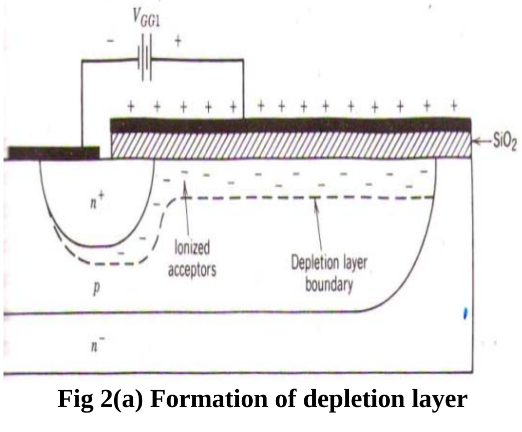


Fig 2(a) Formation of depletion layer

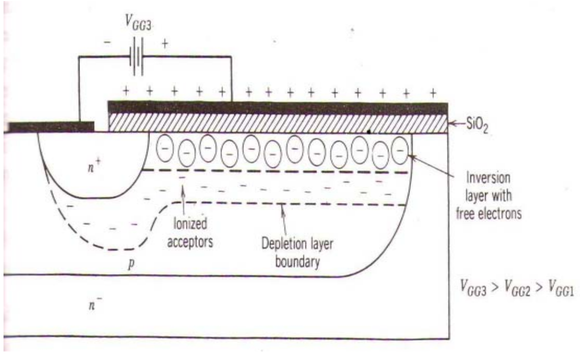
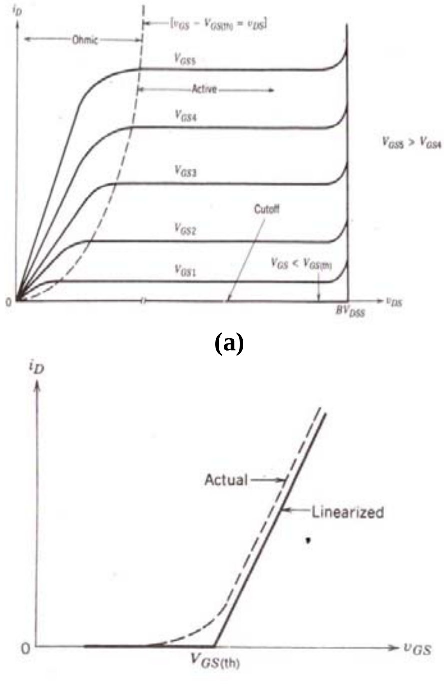


Fig 2(b) Inversion layer at the Si-SiO$_2$ interface as the gate-source voltage is increased

Now a small voltage V_{DD} is applied assuming that V_{GS} is greater than V_{GS}(th), a small value of drain current I_D is produced and the device will be in the ohmic region. The I_D verses V_{DS} characteristics is shown in figure 3(a). Now V_{DD} is slowly increased to ever larger values keeping V_{GS} constant. The drain current will increase in proportion to the increases in V_{DD} since the inversion layer appears as an ohmic resistance connecting the drain to the source. The decrease in the oxide voltage from source to the drain when I_D is flowing reduces the thickness of the inversion layer from source to the drain. As the inversion layer things out, its resistance increases and the curve of I_D versus V_{DS} for a constant V_{GS} begins to flatten out as shown in figure 3(a). The larger the drain current becomes, the flatter the I_D versus V_{DS} characteristics,as shown in figure 3(b).



(a)

(b)

Fig 3 Current-voltage characteristics of a n-channel power MOSFET (a) I_D-V_{DS} characteristics(b) Transfer characteristics

Advantages:

(i) MOSFET is a majority carrier device, hence no storage. Its operating frequency is very high even higher than 100 KHz due to fast turning -on and off.

(ii) Its on-state resistance has a positive temperature coefficient, which makes easy to parallel MOSFETS for increasing current handling capability.

(iii) The safe operating area (SOA) is large (rectangular) because it is not subjected to second breakdown. Therefore, snubber circuits are not needed in most situations.

4.2 CoolMos

Basic Structure

The major drawback of high voltage power MOSFET is the high on –state resistance which is dominated by the resistance of its voltage sustaining drift zone. The voltage blocking capacity of this region is determined by its thickness and the doping.

The COOLMOS concept offers a new approach to reduce the on-state resistance. Figure 4(a) shows a cross section of a COOLMOS.

Operation:

The operation of device under forward biased condition is similar to that of power MOSFET. The current is contributed by the majority carriers only. Because there is no bipolar current contribution, the switching losses are equal to that of power MOSFET. When the device is reversed biased, a lateral electric field is built up, which drives the charge toward the contact regions. The space charge layer builds up along the physical p-n junction line and spreads at a voltage of around 50V across the whole p-n stripped structure. The drift zone is now completely depleted and acts like the voltage sustaining layer of a p-n structure. If the voltage is further increased, the electric field rises linearly without any further expansion of the space charge layer. The current flows through the space charge layer. Both the carrier types are driven toward the contacts by very low electric fields within their columns. This behaviour is a characteristic for charge compensated devices and leads to extremely low losses. This gives an almost linear relationship between the on-state resistance and the maximum blocking voltage

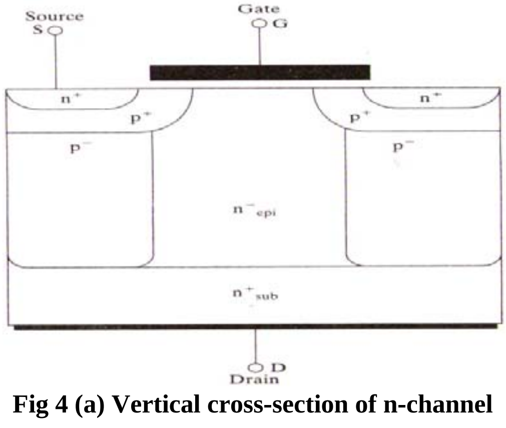


Fig 4 (a) Vertical cross-section of n-channel

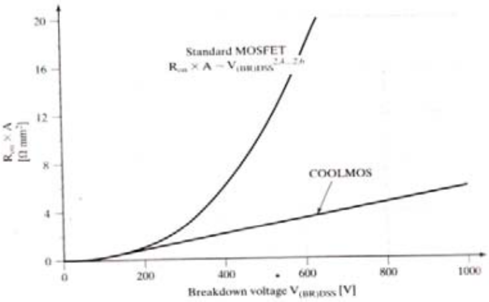


Fig 4(b) Relationship between blocking COOLMOS voltage and on-state resistance

Advantages:

(i) It has lower on-state resistance for the same package as of other MOSFET.

(ii) The conduction losses are atleast five times less as compared with those of the conventional MOSFET technology.

(iii) It is capable of handling two to three times more output power as compared with that of conventional MOSFET.

4.3. Mos – Controlled Thyristor (MCT)

Basic Structure

The MOS-controlled thyristor, is a thyristor like trigger into conduction device that can be turned -on or 0ff by a short pulse on the MOS gate. Because the device can be turned -on and off from the gate terminal, it shares the appealing controllability characteristics of gate turn off (GTO) thyristor while the turn off current gain is very high. The device combines the desirable forward conduction properties of a regenerative four layer thyristor with the high input impedance characteristics of a MOS-controlled gate structure. There are two types of MCTs, the P-MCT and the N-MCT and both combine the low on –state losses and large current capability of thyristors with the advantages of MOS-controlled turn on and turn off and relatively fast switching speeds. The basic structure of a single cell P- MCT the device symbol and equivalent circuit in Figure 5(b). a complete P-MCT is composed of many thousands of these cells fabricated integrally on the same silicon wafer and all the cells are connected electrically in parallel . The two transistor analogy for illustrating the switching is shown in Figure 5(b).

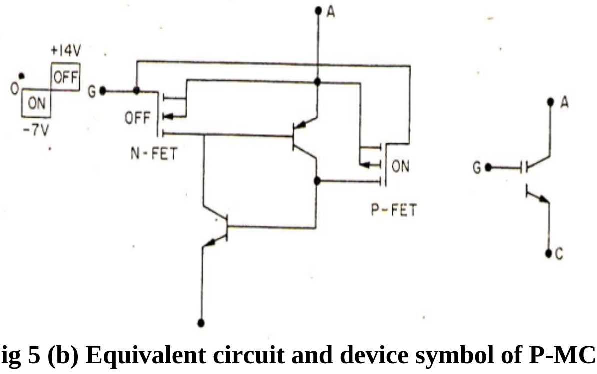


Fig 5 (b) Equivalent circuit and device symbol of P-MCT

Principle of Operation

When a forward, voltage is applied on the anode, the junction J_2 is reverse biased. The applied voltage is blocked mainly by the lightly doped P^- wide base layer. A small reverse saturation current flows through the device. As the on-state resistance of P-Channel FET is much higher than the lateral resistance of the device, most of the current goes directly from anode to cathode leading P-channel FET in operative during conduction, thus, gate loses its control. A short negative voltage pulse (- 7V) is therefore necessary to turn the device on.

If the device is to be turned -off, the gate voltage is made positive with respect to anode. It induces a N- channel below the gate, which short circuits the emitter-base P^+-N junction of upper PNP transistor. The device has large safe operating area and snubberless operation. In the reverse direction, the junctions J_1 and J_3 are reverse biased. The most of the reverse voltage is blocked by junction J_1 which has limited blocking capability because of this N^+ substrate layer. The V-I characteristic of the device is similar to the conventional thyristor except a low break down voltage in the reverse direction.

4.4. Static Induction Transistor (SIT)

A SIT is a high power high frequency device and is essentially a solid state version of a triode vacuum tube. The device was commercially introduced by Tokin Corporation of Japan in 1987. Figure 6(a) shows a basic structure of SIT and its symbol. It is a short N-channel vertical device where the gate electrodes are buried with the drain and source N^-type epi layers. The device is normally on type i.e. if $V_{GS} = 0$, the majority carrier FET like drift current will flow between the drain and the source and the channel resistance will cause conduction drop in the channel. If V_{GS} is negative, the depletion layer of the reverse biased P^+ N junction will inhibit the flow of drain current and with higher bias the channel will be cut-off completely. In the active region, the device V-I characteristics are non-saturating vacuum triode like instead of JFET like The positive temperature coefficient characteristic of channel resistance permits parallel operation of devices. The device applications include AM/FM transmitters, induction heaters, high voltage low current power supplies, ultrasonic generators and linear power amplifiers.

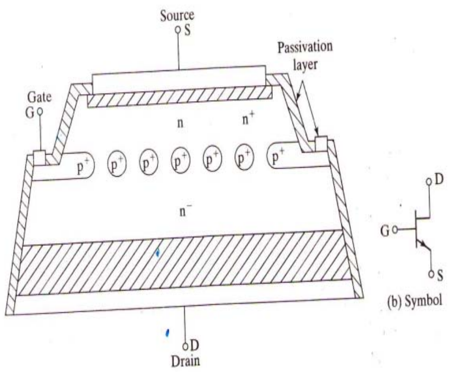


Fig 6(a) Vertical cross-section and symbol of SIT

4.5 Static Induction Thyristor (SITH)

A SITH is a self controlled GTO like on-off device.It is essentially a P^+N N^+ diode with a burried P^+ grid like gate structure. The device structure is similar to SIT except that a P^+ layer has been added to the anode side. Similar to a SIT, it is a normally on device i.e. if the anode is positive and the gate voltage is zero, the device will behave like a diode and anode current will flow freely. The forward biasing of the P^+ N junction will cause a hole injection into the N region and its conductivity is modulated. If the gate is reverse biased with respect to cathode, a depletion layer will block the anode current flow.

The device has applications in induction heating high frequency link dc-dc converter, active power line conditioners and noise-less PWM inverter drives.

CONCLUSION:

The application of SCR will be limited to bulk power control (high voltage and high current) particularly in HVDC, static var compensators etc. Inverter grade thyristors have no future. GTO will be dominating for medium power applications. However, IGCT has bright future and may replace GTO if technology advances. Power Transistor is becoming obsolete. IGBT has replaced power transistor in majority of applications. IGBT will be dominating in medium power control particularly in dc-ac inverters.

REFERENCES

[1] **B.J. Baliga,** "Modern Power Devices" Wiley, New York, 1987.
[2] **Bimal K. Bose**, "Recent Advances in Power Electronics" IEEE Trans. on Power Electronics, Vol. 7, No. 1, Jan. 1992.
[3] **Bimal K. Bose**, "Modern Power Electronics and AC Drives" Pearson Education, New Jersey, 2002.
[4] **V.A.K. Temple**, "MOS-Controlled Thyristors – A new class of Power Devices" IEEE Trans. of Electron Devices, Vol. 33, No. 10, 1986.
[5] **Ned Mohan, T.M. Undeland, W.P. Robbins**, "Power Electronics: Converters, Applications and Design" Wiley India,, 2008.
[6] **M.H. Rashid,** "Power Electronics: Circuits, Devices and Applications, Prentice Hall of India, 2004.
[7] **M.S. Jamil Asghar**, "Power Electronics", Prentice Hall of India, 2005.
[8] **M.D. Singh and K.B. Khanchandani**, "Power Electronics", Tata McGraw Hill Education, 2011.